Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VOUT (2 pads)**
2. **Vin (2 pads)**
3. **ADJUST**
4. **VOUT SENSE**
5. **N/C**
6. **N/C**
7. **N/C**
8. **N/C**

**.086”**

**MASK**

**REF**

**1 4**

**1**

**3**

**1**

**3**

**7**

**A**

**2 2**

**5**

**6**

**7**

**8**

**NOTES:**

**For operation to specification, the chip back MUST be connected to VIN**

For 3 pin applications, connect VOUT SENSE to VOUT

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VIN (See Notes)**

**Mask Ref: 137A**

**APPROVED BY: DK DIE SIZE .086” X .106” DATE: 10/20/21**

**MFG: NATIONAL SEMI THICKNESS .010 P/N: LM137**

**DG 10.1.2**

#### Rev B, 7/19/02